SWARNANDHRA
COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
Accredited by National Board of Accreditation, AICTE, New Delhi,Accredited by NAAC with "A" Grade – 3.32 CGPA,Recognized under 2(f) & 12(B) of UGC Act 1956, Approved by AICTE, New Delhi,Permanent Affiliation to JNTUK, Kakinada
Seetharampuram, W.G.DT., Narsapur-534280, (Andhra Pradesh)

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

TEACHING PLAN

Course Code	Course Title	Semester	Branch	Contact Periods /Week	Academic Year	Date of commencement of Semester
16CS4T03	COMPUTER ORGANIZATION	IV	CSE	5	2019-2020	25.11.2019

COURSE OUTCOMES	
1	Define the Basic functional units and operations of a digital computer(K1)
2	Describe the register transfer language and the analyze Micro operations such as Arithmetic, Shift and Logic micro operations(K2)
3	Define appropriate addressing modes and instructions for writing programs(K1)
4	Explain the different Arithmetic Algorithms, Flowcharts and need for using peripheral devices for efficient operation of system.(K3)
5	Study the different ways of communicating with I/O devices and standard I/O interfaces.(K4)
6	Explain the need for pipeline and storage hierarchy to achieve performance.(K4)

UNIT	CO	Topics No.	Topics/Activity	Text Book / Reference	Contact Hour	Delivery method
I	Define the Basic functional units and operations of a digital	1.01	**Basic Structure of Computers: Basics of computer**	T1,T2	1	Chalk & Talk
		1.02	**Von Neumann Architecture**	T1,T2	1	Chalk & Talk
		1.03	**Generation of Computers**	T1,T2	1	Chalk & Talk
		1.04	**Types of Computers**	T1,T2	1	Chalk & Talk
		1.05	**Functional unit**	T1,T2	1	PPT,Video
		1.06	**Basic Operational Concepts**	T1,T2	1	Chalk & Talk
		1.07	**Bus Structures**	T1,T2	1	PPT,Videos
			Total		07	

II	Describe the register transfer language and the analyze Micro operations such as Arithmetic, Shift and Logic micro operations(K2)	2.01	**Register Transfer Language and Micro Operations: Register Transfer language.**	T1,R1	1	PPT
		2.02	**Register Transfer Bus**	T1,R1	1	Chalk & Talk
		2.03	**Memory transfers**	T1,R1	1	Chalk & Talk
		2.04	**Arithmetic Micro operations**	T1,R1	1	PPT
		2.05	**Logic micro operations**	T1,R1	1	Chalk & Talk
		2.06	**Shift micro operations**	T1,R1	1	PPT
		2.07	**Arithmetic logic shift unit**	T1,R1	1	PPT
		2.08	**Basic Computer Organization and Design: Instruction codes**	T1,R1	1	PPT
		2.09	**Computer Registers**	T1,R1	1	PPT
		2.10	**Computer Instructions**	T1,R1	1	PPT
		2.11	**Timing and control**	T1,R1	1	Chalk & Talk
		2.12	**Instruction Cycle**	T1,R1	1	PPT
		2.13	**Memory – Reference**	T1,R1	1	PPT
		2.14	**Input – Output and Interrupt Instructions**	T1,R1	1	PPT
		2.15	**Design of basic computer**	T1,R1	1	PPT
		2.16	**Design of Accumulator logic**	T1,R1	1	Chalk & Talk
				Total	16	

III	Define appropriate addressing modes and instructions for writing programs(K1)	3.01	**Central Processing Unit: General Register Organization**	T1	1	PPT
		3.02	**STACK organization.**	T1	1	Chalk & Talk
		3.03	**Instruction formats.**	T1	1	video
		3.04	**Addressing modes.**	T1	1	PPT
		3.05	**DATA Transfer and manipulation**	T1	1	PPT
		3.06	**Program control**	T1	1	PPT
		3.07	**Reduced Instruction Set Computer.**	T1	1	PPT
		3.08	**Micro Programmed Control: Control Memory**	T1	1	Chalk & Talk
		3.09	**Address sequencing,**	T1	1	PPT
		3.10	**Micro program example**	T1	1	Chalk & Talk
		3.11	**Design of control unit.**	T1	1	PPT
		Course beyond the syllabus	**Hardware Description Languages**	T1	1	PPT, Videos

			Total		**12**	
IV	Explain the different Arithmetic Algorithms, Flowcharts and need for using peripheral devices for efficient operation of system (K3)	4.01	**Computer Arithmetic: Addition and Subtraction with Signed – Magnitude data**	T1	1	Chalk & Talk
		4.02	**Addition and Subtraction with Signed-2's Complement Data**	T1	1	Chalk & Talk
		4.03	**Multiplication algorithms: Hardware Implementation and Algorithm**	T1	1	PPT
		4.04	**Booth Multiplication Algorithm**	T1	1	Chalk & Talk
		4.05	**Division Algorithms: Hardware Implementation**	T1	1	PPT, Videos
		4.06	**Divide Over flow, Hardware Algorithm**	T1	1	Chalk & Talk
		4.07	**Floating point arithmetic operations: Basic Considerations, Register Configuration**	T1	1	PPT, Videos
		4.08	**Addition and Subtraction**	T1	1	PPT, Videos
		4.09	**Multiplication, Division**	T1	1	PPT, Videos
		4.10	**Decimal Arithmetic unit**	T1	1	PPT, Videos
		4.11	**Decimal arithmetic operations: Addition and subtraction, Multiplication and Division**	T1	1	PPT
		4.12	**Floating –point operations**	T1	1	Chalk & Talk
			Total		**12**	

V	Study the different ways of communicating with I/O devices and standard I/O interfaces.(K4)	5.01	**Input- Output Organization: Peripheral Devices**	T1	1	Chalk & Talk
		5.02	**Input-Output Interface,**	T1	1	Chalk & Talk
		5.03	**Asynchronous data transfer**	T1	1	Chalk & Talk
		5.04	**Modes of Transfer**	T1	1	PPT
		5.05	**Priority Interrupts**	T1	1	Chalk & Talk
		5.06	**Direct memory Access.**	T1	1	Chalk & Talk
		5.07	**The Memory System: Memory Hierarchy Main Memory**	T1	1	PPT,Videos
		5.08	**Auxiliary memory,**	T1	1	PPT
		5.09	**Associative Memory**			
		5.10	**Cache Memory and**	T1	1	PPT
		5.11	**Virtual Memory**	T1	1	Chalk & Talk
		Course Beyond the Syllabus	**IOP**	T1	1	PPT,Videos
				Total	**12**	
VI	Explain the need for pipeline and storage hierarchy to achieve performance.(K4)	6.01	**Parallel Processing and Vector Processing: Parallel Processing**	T1	1	PPT
		6.02	**Pipelining**	T1	1	Chalk & Talk
		6.03	**Arithmetic Pipeline**	T1	1	Chalk & Talk
		6.04	**Instruction Pipeline: Data Dependency**	T1	1	Chalk & Talk
		6.05	**Handling of Branch Instructions**	T1	1	Chalk & Talk
		6.06	**RISC Pipeline: Delayed Load, Delayed Branch**	T1	1	PPT,Videos
		6.07	**Vector Processing: Vector Operations,Matrix Multiplication**	T1	1	PPT,Videos
		6.08	**Memory Interleaving, Superscalar Processors**	T1	1	PPT, videos
		6.09	**Super Computers**	T1	1	Chalk & Talk
		6.10	**Array Processors**	**T1**	1	PPT
				Total	**11**	
			CUMULATIVE PERIODS		**70**	

Text Books:

S.No.	AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION
1.	M.Moris Mano, Computer System Organization, 3rd Edition, Pearson / PHI,2008
2.	Carl Hamacher, Zvonks Vranesic, Safea Zaky, Computer Organization, 5th Edition, McGraw Hill.-2011

3.	John L.Hennessy and David A.Patterson, Computer Organization, a quantitative approach, - Fourth ,Edition Elsevier-2017
Reference Books:	
S.No.	**AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION**
1.	William Stallings,Computer Organization and Architecture- Sixth Edition, Pearson / PHI-2006
2.	Andrew s. Tanenbaum ,Structured Computer Organization -4th Edition, PHI/ Pearson.-2012
3.	Sivaraama Dandamudi ,Fundamentals of Computer Organization and Design - Springer Int. Edition.-2006
Web Details	
1.	https://en.wikibooks.org/wiki/IB/Group_4/Computer_Science/Computer_Organisation
2.	http://www.cs.uwm.edu/classes/cs458/Lecture/HTML/ch05.html
3.	http://www.cse.iitm.ac.in/~vplab/courses/comp_org.html

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vi.	Programme Coordinator	DR P SRINIVASULU	

Principal